Docket No. H1494

DAMASCENE FINFET GATE WITH SELECTIVE METAL INTERDIFFUSION

TECHNICAL FIELD

[0001] The present invention relates generally to transistors and, more particularly, to fin field effect transistors (FinFETs).

BACKGROUND ART

[0002] The escalating demands for high density and performance associated with ultra large scale integration semiconductor devices require design features, such as gate lengths, below 100 nanometers (nm), high reliability and increased manufacturing throughput. The reduction of design features below 100 nm challenges the limitations of conventional methodology.

[0003] For example, when the gate length of conventional planar metal oxide semiconductor field effect transistors (MOSFETs) is scaled below 100 nm, problems associated with short channel effects, such as excessive leakage between the source and drain, become increasingly difficult to overcome. In addition, mobility degradation and a number of process issues also make it difficult to scale conventional MOSFETs to include increasingly smaller device features. New device structures are, therefore, being explored to improve FET performance and allow further device scaling.

[0004] Double-gate MOSFETs represent structures that have been considered as candidates for succeeding existing planar MOSFETs. In double-gate MOSFETs, two gates may be used to control short channel effects. A FinFET is a double-gate structure that exhibits good short channel behavior. A FinFET includes a channel formed in a vertical fin. The FinFET structure may be fabricated using layout and process techniques similar to those used for conventional planar MOSFETs.

DISCLOSURE OF THE INVENTION

[0005] Implementations consistent with the present invention provide a FinFET that includes a gate having layers of different metal materials. In some implementations, a metal material in a first layer of the FinFET gate may be selected such that it has a different work function

than a second metal material in a second layer of the FinFET gate. Due to the diffusivity of the second metal material in the first metal material, after annealing, the second metal material may selectively diffuse through the first metal material. The use of different metals for forming adjacent gate layers over a fin may effectively create two FinFET devices with different threshold voltages (V_t). The first metal material may be associated with a first threshold voltage (V_{t1}) and the second metal material may be associated with a second threshold voltage (V_{t2}). Selective metal interdiffusion, thus, creates two adjacent gate electrode layers for a FinFET that have different gate work functions and which, in turn, have different voltage thresholds (V_t). A FinFET device with multiple voltage thresholds permits the optimization of drive current and/or leakage current for different circuit paths.

[0006] Additional advantages and other features of the invention will be set forth in part in the description which follows and, in part, will become apparent to those having ordinary skill in the art upon examination of the following, or may be learned from the practice of the invention. The advantages and features of the invention may be realized and obtained as particularly pointed out in the appended claims.

[0007] According to the present invention, the foregoing and other advantages are achieved in part by a fin field effect transistor. The fin field effect transistor includes a fin that further includes a channel, a source region formed adjacent a first end of the fin, and a drain region formed adjacent a second end of the fin. The fin field effect transistor further includes a first layer of metal material that includes a first gate electrode, where the first layer of metal material is formed adjacent the fin. The fin field effect transistor also includes a second layer of metal material formed adjacent the first layer, where the second layer of metal material includes a second gate electrode and where the first layer of metal material includes a different work function than the second layer of metal material. The second layer of metal material is further selectively diffused into the first layer of metal material via metal interdiffusion.

[0008] According to another aspect of the invention, a method of forming a multiple voltage threshold fin field effect transistor (finFET) is provided. The method includes forming a fin and forming a source region adjacent a first end of the fin and a drain region adjacent a second end of the fin. The method further includes forming a dummy gate that includes a first material in a first pattern over the fin and forming a dielectric layer adjacent sides of the dummy gate. The method also includes removing the first material to form a trench in the dielectric layer corresponding to the first pattern and forming a first metal gate layer in the trench, where the first metal gate layer includes a first metal material. The method additionally includes forming a second metal gate layer in the trench adjacent the first metal gate layer, where the second metal gate layer includes a second metal material and where the second metal material selectively diffuses through the first metal material via metal interdiffusion to produce a multiple voltage threshold finFET.

[0009] Other advantages and features of the present invention will become readily apparent to those skilled in this art from the following detailed description. The embodiments shown and described provide illustration of the best mode contemplated for carrying out the invention. The invention is capable of modifications in various obvious respects, all without departing from the invention. Accordingly, the drawings are to be regarded as illustrative in nature, and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Reference is made to the attached drawings, wherein elements having the same reference number designation may represent like elements throughout.

[0011] FIG. 1 illustrates exemplary layers of a silicon-on-insulator (SOI) wafer that may be used for forming a fin of a FinFET consistent with the present invention;

[0012] FIG. 2A illustrates an exemplary fin consistent with the invention;

[0013] FIGS. 2B and 2C illustrate source and drain regions formed adjacent the fin of FIG. 2A consistent with the invention;

[0014] FIG. 2D illustrates a cross-sectional view of the exemplary fin of FIG. 2A consistent with the invention;

[0015] FIGS. 3A and 3B illustrate cross-sectional views of dummy oxide and a polysilicon layer formed over the fin of FIG. 2B consistent with the invention;

[0016] FIGS. 4A and 4B illustrate the formation of a dummy gate from the polysilicon layer of FIG. 3B consistent with the invention;

[0017] FIG. 5 illustrates the formation of a dielectric layer adjacent the dummy gate of FIGS. 4A and 4B consistent with the present invention; and

[0018] FIG. 6 illustrates the removal of the dummy gate of FIGS. 4A and 4B to form a gate trench consistent with the present invention;

[0019] FIG. 7 illustrates formation of gate insulation within the gate trench of FIG. 6 consistent with the present invention;

[0020] FIGS. 8A, 8B and 8C illustrate formation of a first metal gate layer within the gate trench of FIG. 7 consistent with the present invention;

[0021] FIGS. 9A and 9B illustrate formation of a photoresist layer over the first metal gate layer of FIGS. 8A, 8B and 8C consistent with the invention;

[0022] FIG. 10 illustrates etching of the first metal gate layer of FIGS. 9A and 9B consistent with the invention;

[0023] FIGS. 11A, 11B and 11C illustrate formation of a second metal gate layer within the gate trench of FIGS. 8A, 8B and 8C consistent with the present invention;

[0024] FIG. 12 illustrates formation of a crystalline silicon layer consistent with another embodiment of the invention;

[0025] FIG. 13 illustrates formation of an oxide layer and an amorphous silicon layer over the crystalline silicon layer of FIG. 12 consistent with the other embodiment of the invention;

[0026] FIG. 14 illustrates formation of an oxide layer on the amorphous silicon layer of FIG. 13 consistent with the other embodiment of the invention; and

[0027] FIG. 15 illustrates formation of a stacked merged FET via metal induced crystallization consistent with the other embodiment of the invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0028] The following detailed description of the invention refers to the accompanying drawings. The same reference numbers in different drawings may identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and their equivalents.

[0029] Consistent with the present invention, an exemplary damascene process for forming a FinFET is provided. In the exemplary damascene process, a dummy gate may be formed from a layer of semi-conducting material, such as, for example, polysilicon, that has been formed over a fin. A dielectric layer may then be formed over the FinFET fin, source and drain regions around the dummy gate. The dummy gate may then be removed to create a gate trench in the dielectric layer. A first layer of a first metal material may be formed within the gate trench. A second layer of a second metal material may be formed within the gate trench adjacent the first layer. The first metal material and the second metal material may have different work functions such that, after metal interdiffusion of the second metal material into the first metal material, a FinFET device with different threshold voltages (V_t) may be created, with the first metal material being associated with a first threshold voltage (V_{t1}) and the second metal material being associated with a second threshold voltage (V_{t2}).

[0030] FIG. 1 illustrates a cross-section of a silicon-on-insulator (SOI) wafer 100 formed in accordance with an exemplary embodiment of the present invention. SOI wafer 100, consistent with the present invention, may include a buried oxide layer 110 formed on a substrate 115. A fin layer 105 may further be formed on buried oxide layer 110. The thickness of fin layer 105 may range, for example, from about 500Å to about 2000Å and the thickness of buried oxide layer 110 may range, for example, from about 1000Å to about

3000Å. Fin layer 105 and substrate 115 may include, for example, silicon, though other semi-conducting materials, such as germanium, may be used.

[0031] As shown in FIGS. 2A and 2D, a vertical fin 205 may be formed from fin layer 105. Fin 205 may be formed, for example, with a width (w) in a range of 10-15 nm. Fin 205 may be formed from fin layer 105 using any conventional process, including, but not limited to, conventional photolithographic and etching processes.

[0032] Subsequent to formation of fin 205, source 210 and drain 215 regions may be formed adjacent respective ends of fin 205, as shown in FIGS. 2B and 2C. Source 210 and drain 215 regions may be formed by, for example, deposition of a layer of semi-conducting material over fin 205. The source 210 and drain 215 regions may be formed from the layer of semi-conducting material using, for example, conventional photolithographic and etching processes. One skilled in the art will recognize, however, that other existing techniques may be used for forming source 210 and drain 215 regions. For example, source 210 and drain 215 regions may be formed by patterning and etching fin layer 105. Source 210 and drain 215 regions may include a semi-conducting material such as, for example, silicon, germanium or silicon-germanium (Si-Ge). In one implementation, $Si_xGe_{(1-x)}$, with x approximately equal to 0.7 may be used. A cap 220 may then be formed on upper surfaces of fin 205, source 210 and drain 215, as illustrated in FIG. 2D. Cap 220 may include an oxide, such as, for example, silicon oxide, and may range, for example, from about 100Å to about 500Å in thickness.

[0033] After formation of source 210 and drain 215 regions, dummy oxide 305 may be formed on fin 205, source 210 and drain 215 using a conventional process, as shown in FIG. 3A. Dummy oxide 305, for example, may be thermally grown on fin 205, source 210 and drain 215. Dummy oxide 305 may include an oxide, such as, for example, silicon oxide and may range, for example, from about 100Å to about 500Å in thickness.

[0034] As further shown in FIG. 3B, a layer of polysilicon 310 may be formed over fin 205, source 210 and drain 215. The thickness of polysilicon layer 310 may range, for example, from about 500Å to about 2000Å. Polysilicon layer 310 may be polished back using, for example, a chemical-mechanical polishing (CMP) process, to achieve a planar surface to improve subsequent gate lithography. As shown in FIGS. 4A and 4B, a dummy gate 405 may be defined in polysilicon layer 310 using a conventional process, such as, for example, a conventional patterning and etching process.

[0035] As shown in FIG. 5, a dielectric layer 505 may be formed over dummy gate 405 using, for example, conventional deposition processes. Dielectric layer 505 may include, for example, tetraethylorthosilicate (TEOS), or any other dielectric material. The thickness of dielectric layer 505 may range, for example, from about 100Å to about 300Å. Dielectric layer 505 may then be polished back to the upper surface of dummy gate 405 using, for example, a CMP process, as illustrated in FIG. 5.

[0036] Dummy gate 405 and dummy oxide 305 may then be removed, as shown in FIG. 6, leaving a gate trench 605. Dummy gate 405 and dummy oxide 305 may be removed using, for example, conventional etching processes. Gate insulation 705 may then be formed in gate trench 605, as shown in FIG. 7. Gate insulation 705 may be thermally grown or deposited using conventional deposition processes. Gate insulation 705 may include SiO, SiO_2, SiN, SiON, HFO_2, ZrO_2, Al_2O_3, HFSiO(x) ZnS, MgF_2, or other high-K dielectric materials. The thickness of gate insulation layer 705 may range, for example, from about 10Å to about 50Å.

[0037] As shown in FIGS. 8A, 8B and 8C, a first metal material 805 may be formed in gate trench 605 over gate insulation 705. Metal material 805 may be formed in gate trench 605 using a conventional metal deposition process. Metal material 805 may include a metal material, such as, for example, Ti or Ni, though other metal materials may alternatively be used. The thickness of metal material 805 may range, for example, from about 300Å to about 1000Å.

[0038] As further shown in FIGS. 9A and 9B, a photoresist pattern 905 may be formed over gate material 805. Using a conventional etching process, metal material 805 may be etched to form a first gate electrode 1005, as shown in FIG. 10. Photoresist pattern 905 may then be removed from first gate electrode 1005.

[0039] As shown in FIGS. 11A, 11B and 11C, a second metal material 1105 may be formed in gate trench 605 over first gate electrode 1005 to form a second gate electrode. Metal material 1105 may be formed in gate trench 605 using a conventional metal deposition process. Metal material 1105 may include a metal material, such as, for example, Ni or Ti, though other metal materials may alternatively be used. The thickness of metal material 1105 may range, for example, from about 300Å to about 1000Å.

[0040] Metal material 1105 may be selected such that it has a different work function than first metal material 805. For example, in one implementation, second metal material 1105 may be selected with a high work function, whereas first metal material 805 may be selected with a low work function. Due to diffusivity of the second metal material 1105 in the first metal material 805, after annealing, the second metal material 1105 may selectively diffuse through the first metal material to gate insulation 705. The use of different metals for forming adjacent gate electrodes over a fin may effectively create two FinFET devices with different threshold voltages (V_t). The first metal material 805 may be associated with a first threshold voltage (V_{t1}) and the second metal material 1105 may be associated with a second threshold voltage (V_{t2}). Selective metal interdiffusion, thus, achieves different gate work functions for different gate electrodes of a FinFET which, in turn, produces different voltage thresholds (V_t). A FinFET device with multiple voltage thresholds permits the optimization of drive current and/or leakage current for different circuit paths.

EXEMPLARY SELF-STOPPING POLY PLANARIZATION

[0041] FIGS. 12-15 illustrate an exemplary process for forming a stacked merged FET using metal induced crystallization, consistent with another embodiment of the present invention.

As shown in FIG. 12, the exemplary process may begin with the formation of a layer 1205 of amorphous silicon (α-Si) material. Layer 1205 may be formed, for example, using conventional deposition processes and may range, for example, from about 300Å to about 1000Å in thickness. The amorphous silicon of layer 1205 may then be annealed to convert the amorphous silicon to crystalline silicon via metal induced crystallization (MIC). Subsequent to MIC, layer 1205 may be implanted with an *n* channel material 1210 to produce an *n* type FET channel. *n* channel material 1210 may include, for example, Si, Ge, or SiGe, and may be implanted to a doping/concentration level that may range, for example, from about $10^{15}cm^{-3}$ to about $10^{17}cm^{-3}$.

[0042] Subsequent to *n* channel implantation, an oxide layer 1305 may be formed on layer 1205, as shown in FIG. 13. Oxide layer 1305 may include an oxide, such as, for example, silicon oxide and may range, for example, from about 300Å to about 1000Å in thickness. In one implementation, for example, oxide layer 1305 may be thermally grown on layer 1205. A layer 1310 of amorphous silicon (α-Si) material may then be formed on oxide layer 1305. Layer 1310 may be formed, for example, using conventional deposition processes and may range, for example, from about 300Å to about 1000Å in thickness. Subsequent to formation, layer 1310 may be implanted with a *p* channel material 1315, such as, for example, Si, Ge, or SiGe, to a doping/concentration level that may range, for example, from about $10^{15}cm^{-3}$ to about $10^{17}cm^{-3}$.

[0043] As shown in FIG. 14, an oxide layer 1405 may be formed on layer 1310. Oxide layer 1405 may include an oxide, such as, for example, silicon oxide and may range, for example, from about 300Å to about 1000Å in thickness. In one implementation, for example, oxide layer 1405 may be thermally grown on layer 1310. Layers 1205, 1305, 1310 and 1405 may then be formed into a stack, as shown in FIG. 14, using a conventional patterning and etching process.

[0044] The amorphous silicon of layer 1310 may then be annealed to convert the amorphous silicon to crystalline silicon, via MIC, to produce a *p*-type crystalline silicon layer 1510, as illustrated in FIG. 15. Creation of the *n*-type crystalline silicon layer 1205 and the *p*-type crystalline silicon layer 1510, thus, produces a stacked, merged FET consistent with another embodiment of the invention.

[0045] In the previous descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, the present invention can be practiced without resorting to the details specifically set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention. In practicing the present invention, conventional photolithographic, etching and deposition techniques may be employed, and hence, the details of such techniques have not been set forth herein in detail.

[0046] The foregoing description of embodiments of the present invention provides illustration and description, but is not intended to be exhaustive or to limit the invention to the precise form disclosed. Modifications and variations are possible in light of the above teachings or may be acquired from practice of the invention. For example, while series of acts has been described above, the order of the acts may vary in other implementations consistent with the present invention.

[0047] Only the preferred embodiments of the invention and a few examples of its versatility are shown and described in the present disclosure. It is to be understood that the invention is capable of use in various other combinations and environments and is capable of modifications within the scope of the inventive concept as expressed herein. No element, act, or instruction used in the description of the present application should be construed as critical or essential to the invention unless explicitly described as such. Also, as used herein, the article "a" is intended to include one or more items. Where only one item is intended, the

term "one" or similar language is used. The scope of the invention is defined by the following claims and their equivalents.